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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,154	12/31/2003	Kuljit S. Bains	42P18551	7899

8791 7590 02/21/2006

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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 02/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/750,154	Applicant(s) BAINS ET AL.	
	Examiner Lev I. Iwashko	Art Unit 2186	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3, 5-8, and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Jung-bae Lee et al. (US Patent 6,151,271).

Claim 1. An memory IC comprising: *(Abstract, lines 1 – Declares integrated circuit memory devices)*

- a first group of banks of memory having a first bank, a first row address decoder coupled to the first bank, and a first bank selection logic coupled to the first row address decoder; *(Figure 1, components 10, 14, and 19A, and Figure 2, components 41 and 44 – All show how the first group of banks of memory are coupled to the first bank selector which is coupled also to the decoder)*
- a second group of banks of memory having a second bank, a second row address decoder coupled to the second bank, and a second bank selection logic coupled to the second row address decoder, all able to operate independently of the first bank, first row address decoder and first bank selection logic; *(Figure 1, components 20, 24, and 19B, and Figure 2, components 43 and 46 – All show how the first group of banks of memory are coupled to the first bank selector which is coupled also to the decoder)*
- control logic shared by both the first and second groups, coupled to both the first and second row address decoders, coupled to both the first and second bank selection logics, storing information concerning

the state of all banks in the first group, including the first bank, and separately storing information concerning the state of all banks in the second group, including the second bank; *(Column 1, lines 66-67 and Column 2, lines 1-16 – State the following: "These and other objects, advantages and features of the present invention are provided by integrated circuit memory devices which include first and second memory banks, first and second local data lines electrically coupled to the first and second memory banks, respectively, and a multiplexer having first and second inputs electrically coupled to first and second data bus lines, respectively. A data selection circuit is also provided which routes data from the first and second local data lines to the first and second data bus lines, respectively, when a selection control signal is in a first logic state and routes data from the second and first local data lines to the first and second data bus lines, respectively, when a selection control signal is in a second logic state opposite the first logic state. A control signal generator is also provided. This control signal generator generates the selection control signal in the first and second logic states when a first address in a string of burst addresses is even and odd, respectively." Column 3, lines 9-44 – State the following: "Referring to FIG. 1, a synchronous DRAM according to a first embodiment of the present invention includes a plurality of memory cell arrays, and each of the memory cell arrays includes a plurality of memory cell subarrays. For convenience, two memory cell subarrays are shown in FIG. 1. In detail, the synchronous DRAM of FIG. 1 includes an even-numbered memory core 10, an odd-numbered memory core 20, an amplifying and a multiplexing circuit 30, an output buffer 31, a control signal generator 32 and a mode register 34. The even-numbered memory core 10 includes a first memory cell subarray 12, a row decoder 14 and a column decoder 16. Each cell of the first memory cell subarray 12 is accessed by a row address and a*

column address decoded by the row decoder 14 and the column decoder 16, respectively, to thereby write data to or read data from the first memory cell subarray 12. The read data is amplified by a bit line sense amplifier 18, and the amplified data is loaded on an even local input and output line 19a. At this time, the column address applied to access the first memory cell subarray 12 is preferably an even-numbered address. The odd-memory core 20 includes a second memory cell subarray 22, a row decoder 24 and a column decoder 26. Each cell of the second memory cell subarray 22 is accessed by a row address and a column address decoded by the row decoder 24 and the column decoder 26, respectively, to thereby read data from or write data to the second memory cell. The read data is amplified by a bit line sense amplifier 28, and the amplified data is loaded on an odd local input and output line 19b. At this time, a column address applied to access the second memory cell subarray 22 is preferably an odd numbered address. Accordingly, a predecoder can be used to delineate between odd numbered addresses when data is to be written to or read from the odd-memory core 20, and even numbered addresses when data is to be written to or read from the even-numbered memory core 10")

- and a data buffer shared by both the first and second groups. *(Column 3, lines 51-53 – State the following: "Data DO is buffered by the output buffer 30 and the buffered data DOUT is output to an external system bus")*

Claim 2. The memory IC of claim 1, wherein the control logic and the data buffer cooperate to couple the memory IC to a memory bus and share access to the memory bus between the first and second groups, *(Figure 1, components 10, 20, 30 and 31 – Show how the buffer and selection control logic couple the memory IC to a memory bus to share access to the first and second groups)*

- with the control logic receiving at least addresses and commands from the memory bus for memory operations involving both the first and second groups, *(Column 7, lines 52-53 – State the following: "a data selection circuit which routes data from the first and second local data lines to the first and second data bus lines, respectively, when a selection control signal is in a first logic state and routes data from the second and first local data lines to the first and second data bus lines, respectively, when the selection control signal is in a second logic state opposite the first logic state. The memory device of claim 1, further comprising a control signal generator which generates the selection control signal in the first and second logic states when a first address in a string of burst addresses is even and odd, respectively")*
- and with the data buffer transferring data between the memory bus and both the first and second groups. *(Column 3, lines 45-54 – Show how the buffer transfers the data between the first (IO_E output from first core) and second (IO_O output from second core) groups and the bus)*

Claim 3. The memory IC of claim 2, wherein the control logic incorporates logic to arbitrate between the first and second groups for access to the data buffer to transfer data to and from the memory bus. (*Column 7, lines 52-58 – State the following: "a data selection circuit which routes data from the first and second local data lines to the first and second data bus lines, respectively, when a selection control signal is in a first logic state and routes data from the second and first local data lines to the first and second data bus lines, respectively, when the selection control signal is in a second logic state opposite the first logic state")*

Claim 5. The memory IC of claim 1, wherein a read transaction to read data from a row within the first bank is able to be timed and carried entirely independently of a read transaction to read data from a row within the second bank. *(Column 3, lines 39-44 – State the following: "Accordingly, a predecoder can be used to delineate between odd numbered addresses*

when data is to be written to or read from the odd-memory core 20, and even numbered addresses when data is to be written to or read from the even-numbered memory core 10")

Claim 6. An electronic system comprising:

- a memory IC having a first group of banks having a first bank, second group of banks having a second bank, control logic shared by both the first and second groups and having both a first state logic storing information concerning the state of all banks in the first group and a second state logic storing information concerning the state of all banks in the second group, *(Column 1, lines 66-67 and Column 2, lines 1-16 – State the following: "These and other objects, advantages and features of the present invention are provided by integrated circuit memory devices which include first and second memory banks, first and second local data lines electrically coupled to the first and second memory banks, respectively, and a multiplexer having first and second inputs electrically coupled to first and second data bus lines, respectively. A data selection circuit is also provided which routes data from the first and second local data lines to the first and second data bus lines, respectively, when a selection control signal is in a first logic state and routes data from the second and first local data lines to the first and second data bus lines, respectively, when a selection control signal is in a second logic state opposite the first logic state. A control signal generator is also provided. This control signal generator generates the selection control signal in the first and second logic states when a first address in a string of burst addresses is even and odd, respectively." Column 3, lines 9-44 – State the following: "Referring to FIG. 1, a synchronous DRAM according to a first embodiment of the present invention includes a plurality of memory cell arrays, and each of the memory cell arrays includes a plurality of memory cell subarrays. For convenience, two memory cell subarrays*

are shown in FIG. 1. In detail, the synchronous DRAM of FIG. 1 includes an even-numbered memory core 10, an odd-numbered memory core 20, an amplifying and a multiplexing circuit 30, an output buffer 31, a control signal generator 32 and a mode register 34. The even-numbered memory core 10 includes a first memory cell subarray 12, a row decoder 14 and a column decoder 16. Each cell of the first memory cell subarray 12 is accessed by a row address and a column address decoded by the row decoder 14 and the column decoder 16, respectively, to thereby write data to or read data from the first memory cell subarray 12. The read data is amplified by a bit line sense amplifier 18, and the amplified data is loaded on an even local input and output line 19a. At this time, the column address applied to access the first memory cell subarray 12 is preferably an even-numbered address. The odd-memory core 20 includes a second memory cell subarray 22, a row decoder 24 and a column decoder 26. Each cell of the second memory cell subarray 22 is accessed by a row address and a column address decoded by the row decoder 24 and the column decoder 26, respectively, to thereby read data from or write data to the second memory cell. The read data is amplified by a bit line sense amplifier 28, and the amplified data is loaded on an odd local input and output line 19b. At this time, a column address applied to access the second memory cell subarray 22 is preferably an odd numbered address. Accordingly, a predecoder can be used to delineate between odd numbered addresses when data is to be written to or read from the odd-memory core 20, and even numbered addresses when data is to be written to or read from the even-numbered memory core 10")

- and a data buffer; *(Column 3, lines 51-53 – State the following: "Data DO is buffered by the output buffer 30 and the buffered data DOUT is output to an external system bus")*

- a memory controller having a third state logic storing information concerning the state of all banks in the first group within the memory IC, and having a fourth state logic storing information concerning the state of all banks in the second group within the memory IC; *(Column 8, lines 13-18 – State the following: "wherein said first and second selectors are responsive to second and third control signals, respectively; wherein said multiplexer is responsive to fourth and fifth control signals; and wherein the fourth and fifth control signals are delayed versions of the second and third control signals, respectively")*
- and a memory bus coupling the control logic and data buffer of the memory IC to the memory controller. *(Figure 1, components 30 and 31 – Show all the above components coupled together by a bus)*

Claim 7. The electronic system of claim 6, wherein the control logic and the data buffer cooperate to share access to the memory bus between the first and second groups, *(Figure 1, components 10, 20, 30 and 31 – Show how the buffer and selection control logic couple the memory IC to a memory bus to share access to the first and second groups)*

- with the control logic receiving at least addresses and commands from the memory bus for memory operations involving both the first and second groups, *(Column 7, lines 52-53 – State the following: "a data selection circuit which routes data from the first and second local data lines to the first and second data bus lines, respectively, when a selection control signal is in a first logic state and routes data from the second and first local data lines to the first and second data bus lines, respectively, when the selection control signal is in a second logic state opposite the first logic state. The memory device of claim 1, further comprising a control signal generator which generates the selection control signal in the first and second logic states when a first address in a string of burst addresses is even and odd, respectively")*

- and with the data buffer transferring data between the memory bus and both the first and second groups. *(Column 3, lines 45-54 – Show how the buffer transfers the data between the first (IO_E output from first core) and second (IO_O output from second core) groups and the bus)*

Claim 8. The electronic system of claim 7, wherein the control logic incorporates logic to arbitrate between the first and second groups for access to the data buffer to transfer data to and from the memory bus. (*Column 7, lines 52-58 – State the following: "a data selection circuit which routes data from the first and second local data lines to the first and second data bus lines, respectively, when a selection control signal is in a first logic state and routes data from the second and first local data lines to the first and second data bus lines, respectively, when the selection control signal is in a second logic state opposite the first logic state")*

Claim 12. The electronic system of claim 6, wherein the control logic permits a read transaction to read data from a row within the first bank is able to be timed and carried entirely independently of a read transaction to read data from a row within the second bank. *(Column 3, lines 39-44 – State the following: "Accordingly, a predecoder can be used to delineate between odd numbered addresses when data is to be written to or read from the odd-memory core 20, and even numbered addresses when data is to be written to or read from the even-numbered memory core 10")*

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 4 and 11 are rejected under 35 U.S.C.103(a) as being unpatentable over Jung-bae Lee as applied to claims 1 and 6 above, further in view of Ho-Cheol Lee (US Patent 6,279,116 B1).

Jung-bae Lee teaches the limitations of claims 1 and 6 for the reasons above.

Jung-bae Lee's invention differs from the claimed invention in that there is no specific reference to control logic storing row availability information.

Jung-bae Lee fails to teach claims 4 and 11, which respectively state the following: "The memory IC of claim 1, wherein the control logic stores information concerning which rows are open in all banks in the first group separately from information concerning which rows are open in all banks in the second group" and "The electronic system of claim 6, wherein the control logic stores information concerning which rows are open in all banks in the first group separately from information concerning which rows are open in all banks in the second group." However, Ho-Cheol Lee states the following: "The row control circuit is means for generating signals or clocks for selecting word lines during the time period of t.sub.RCD, developing to bit lines information data from memory cells in a read operation and precharging during the time period of t.sub.RP. In other words, the row control circuit decides whether or not the rows are open" (Column 13, lines 45-49). Therefore, it would have been obvious to one of ordinary skill in the art to combine the "Integrated Circuit Devices" of Jung-bae Lee and Ho-Cheol Lee's "Synchronous Dynamic Random Access Memory Devices", so that a "control logic" could store information on row availability to make the system more accurate and user-friendly.

5. Claim 9 is rejected under 35 U.S.C.103(a) as being unpatentable over Jung-bae Lee as applied to claim 6 above, further in view of Ho-Cheol Lee (US Patent 6,279,116 B1).

Jung-bae Lee teaches the limitations of claim 6 for the reasons above.

Jung-bae Lee's invention differs from the claimed invention in that there is no specific reference to a cache.

Jung-bae Lee fails to teach claim 9, which states the following: "The electronic system of claim 6, further comprising a processor coupled to the memory controller; and a cache utilized by the processor to store a subset of data stored in the memory IC." However, Ho-Cheol Lee states the following: "To compensate for the gap between the operation speed of the CPU and that of the main memory like the DRAM, the computer system includes an expensive high-speed buffer memory such as a cache memory which is arranged between the CPU and the main memory. The cache memory stores information data from the main memory which is requested by the CPU. Whenever the CPU issues the request for the data, a cache memory controller intercepts it and checks the cache memory to see if the data is stored in the cache memory. If the requested data exists therein, it is called a cache hit, and high-speed data transfer is immediately performed from the cache memory to the CPU. Whereas if there is no presence therein, it is called a cache miss, and the cache memory controller reads out the data from the slower main memory. The read-out data is stored in the cache memory and sent to the CPU. Thus, a subsequent request for this data may be immediately read out from the cache memory. That is, in case of the cache hit, the high-speed data transfer may be accomplished from the cache memory. However, in case of the cache miss, the high-speed data transfer from the main memory to the CPU cannot be expected, thereby incurring wait states of the CPU. Thus, it is extremely important to design DRAMs serving as the main memory to accomplish high-speed operations" (Column 1, lines 50-67 and Column 2, lines 1-6). Therefore, it would have been

obvious to one of ordinary skill in the art to combine the "Integrated Circuit Devices" of Jung-bae Lee and Ho-Cheol Lee's "Synchronous Dynamic Random Access Memory Devices", so that a cache could be utilized for storage making the system more efficient.

6. Claim 10 is rejected under 35 U.S.C.103(a) as being unpatentable over Jung-bae Lee as applied to claims 6 and 9 above, further in view of Carnevale et al. (US Patent 5,721,874).

Jung-bae Lee teaches the limitations of claims 6 and 9 for the reasons above.

Jung-bae Lee's invention differs from the claimed invention in that there is no specific reference to cache size.

Jung-bae Lee fails to teach claim 10, which states the following: "The electronic system of claim 9, wherein the memory controller incorporates a control storage to maintain information concerning the size of a cache line within the cache." However, Carnevale states the following: "FIG. 8 is a block diagram representation illustrating a page table arrangement for storing cache characteristic information for controlling cache access to the configurable caches 12 and 22. A page table 50 stores address information. Each page table entry 52 within the page table 50 includes other page table information 54 and a cache line characteristic data 56. The cache line characteristic data 56 includes the number of address bits to be matched in the cache directory 32 and a cache line size" (Column 4, line 50-59). Therefore, it would have been obvious to one of ordinary skill in the art to combine the "Integrated Circuit Devices" of Jung-bae Lee and Carnevale's "Configurable Cache", so that information about cache size could be maintained to assure system accuracy and reduce chance of information traffic lag.

7. Claim 13 is rejected under 35 U.S.C.103(a) as being unpatentable over Jung-bae Lee as applied to claims 6 and 12 above, further in view of Kopet et al. (US Patent 5,448,310).

Jung-bae Lee teaches the limitations of claims 6 and 12 for the reasons above.

Jung-bae Lee teaches the following limitation of claim 13:

The electronic system of claim 12,

- wherein the memory controller transmits addresses and commands to the memory IC for a first read transaction to read data from a first row within a bank in the first group and for second read transaction to read data from a second row within a bank in the second group, *(Column 7, lines 52-53 – State the following: "a data selection circuit which routes data from the first and second local data lines to the first and second data bus lines, respectively, when a selection control signal is in a first logic state and routes data from the second and first local data lines to the first and second data bus lines, respectively, when the selection control signal is in a second logic state opposite the first logic state. The memory device of claim 1, further comprising a control signal generator which generates the selection control signal in the first and second logic states when a first address in a string of burst addresses is even and odd, respectively")*

Jung-bae Lee's invention differs from the claimed invention in that there is no specific reference to early termination.

Jung-bae Lee fails to teach the following limitation of claim 13:

- wherein the memory controller signals the memory IC that both the first and second read transactions are to be terminated early at a quantity of bytes less than the quantity of bytes that the memory IC normally fetches internally for a read transaction, wherein the memory controller times the first and second read transactions to minimize the time that elapses between the end of the actual transfer of bytes across the memory bus for the first read transaction and the beginning of the actual transfer of bytes across the memory bus for the second read transaction.

However, Kopet states the following: "The differences between Mode 1 and the Mode 0 burst read cycle shown in FIG. 31, are that for the Mode 1 cycle, HMODE is initially set high (instead of low) and there is only a single clock cycle (instead of two clocks) separating one burst access from the next. Just as for a Mode 0 burst read, however, HBRST 800 is asserted

during the burst for every additional word to be accessed after the first word, and MEC 20 asserts HRDY- for every word it asserts on the data bus. However, unlike a Mode 0 burst read, Mode 1 burst reads do not require HBRST 800 to be deasserted during the last access. Also, if HBRST 800 is deasserted during a Mode 1 burst read cycle prior to reading all (BLENGTH+2) words, the burst cycle terminates on the rising edge of the next clock to follow the deassertion. Due to internal pipelining, MEC 20 reads one additional word beyond the point of termination, even though this word is never asserted onto the data bus. An example of such an "early termination," (as opposed to the "normal termination") is depicted in FIG. 33. In FIG. 33, HBRST 800 is deasserted during the HRDY- cycle for "Data 0", causing the burst to be terminated at that point. However, internally MEC 20 still reads "Data 1"" (Column 12, lines 10-34). Therefore, it would have been obvious to one of ordinary skill in the art to combine the "Integrated Circuit Devices" of Jung-bae Lee and Kopet's "Motion Estimation Coprocessor", so that early termination could occur when necessary to make the system more universally user-friendly and efficient.

8. Claims 14 and 15 are rejected under 35 U.S.C.103(a) as being unpatentable over Jung-bae Lee as applied to claims 6, 12, and 13 above, further in view of Kopet et al. (US Patent 5,448,310).

Jung-bae Lee teaches the limitations of claims 6, 12, and 13 for the reasons above.

Jung-bae Lee's invention differs from the claimed invention in that there is no specific reference to early termination.

Jung-bae Lee fails to teach claims 14 and 15, which respectively state the following: "The electronic system of claim 13, wherein the memory controller signals the memory IC that both the first and second read transactions are to be terminated early through indications of early

termination embedded in the commands transmitted to the memory IC for both the first and second read transactions" and "The electronic system of claim 13, wherein the memory controller signals the memory IC that both the first and second read transactions are to be terminated early through transmitting first and second burst termination commands across the memory bus, timed to indicate when to cease transferring further bytes of data for each of the first and second read transactions." However, Kopet states the following: "The differences between Mode 1 and the Mode 0 burst read cycle shown in FIG. 31, are that for the Mode 1 cycle, HMODE is initially set high (instead of low) and there is only a single clock cycle (instead of two clocks) separating one burst access from the next. Just as for a Mode 0 burst read, however, HBRST 800 is asserted during the burst for every additional word to be accessed after the first word, and MEC 20 asserts HRDY- for every word it asserts on the data bus. However, unlike a Mode 0 burst read, Mode 1 burst reads do not require HBRST 800 to be deasserted during the last access. Also, if HBRST 800 is deasserted during a Mode 1 burst read cycle prior to reading all (BLENGTH+2) words, the burst cycle terminates on the rising edge of the next clock to follow the deassertion. Due to internal pipelining, MEC 20 reads one additional word beyond the point of termination, even though this word is never asserted onto the data bus. An example of such an "early termination," (as opposed to the "normal termination") is depicted in FIG. 33. In FIG. 33, HBRST 800 is deasserted during the HRDY- cycle for "Data 0", causing the burst to be terminated at that point. However, internally MEC 20 still reads "Data 1"" (Column 12, lines 10-34). Therefore, it would have been obvious to one of ordinary skill in the art to combine the "Integrated Circuit Devices" of Jung-bae Lee and Kopet's "Motion Estimation

Coprocessor", so that early termination could occur when necessary to make the system more universally user-friendly and efficient.

9. Claim 16 is rejected under 35 U.S.C.103(a) as being unpatentable over Jung-bae Lee, further in view of the non-patent literature "Bit Vector Algorithm for Detecting Self-Data Chains" (hereafter referred to as "IBM").

Jung-bae Lee teaches the following limitations of Claim 16:

A method comprising:

- selecting a first read operation to read data from a first row in a first group of banks in a memory IC; *(Column 3, lines 18-24 – State the following: "The even-numbered memory core 10 includes a first memory cell subarray 12, a row decoder 14 and a column decoder 16. Each cell of the first memory cell subarray 12 is accessed by a row address and a column address decoded by the row decoder 14 and the column decoder 16, respectively, to thereby write data to or read data from the first memory cell subarray 12")*
- selecting a second read operation to read data from a second row in a second group of banks in the memory IC; *(Column 3, lines 30-36 – State the following: "The odd-memory core 20 includes a second memory cell subarray 22, a row decoder 24 and a column decoder 26. Each cell of the second memory cell subarray 22 is accessed by a row address and a column address decoded by the row decoder 24 and the column decoder 26, respectively, to thereby read data from or write data to the second memory cell")*
- transmitting a first read command for the first read operation to the memory IC; *(Column 4, lines 31-35 – State the following: "Alternatively, when an initial column address is odd-numbered during a burst read operation, the selection control signal SEL is low (logic 0). When this occurs, the first data bus selector 44 transfers the odd data FDIO.sub.-- O to the first data bus DB.sub.—F")*
- transmitting a second read command for the second read operation to the memory IC; *(Column 4, lines 43-48 – State the following: "In particular, when an initial column address is even-numbered during a read operation, the complementary selection control signal /SEL is 'low'. At this time, the second data bus selector 46 selects the odd data FDIO.sub.-- O, and transfers the odd data to the second data bus DB.sub.—S")*
- receiving the burst transfer of data for the first read operation from the first row of the first group; *(Column 4, lines 26-28 – State the*

following: "When the SDRAM outputs burst data and the initial column address of the output data is even-numbered, the selection control signal SEL is 'high'")

- and receiving the burst transfer of data for the second read operation from the second row of the second group. *(Column 4, lines 31-33 – State the following: "Alternatively, when an initial column address is odd-numbered during a burst read operation, the selection control signal SEL is low (logic 0)")*

IBM teaches the following limitation of claim 16:

- determining a quantity of bytes to which each transfer of data will be limited for both the first and second read operations; *(Page 3, lines 33-45 and Page 4, lines 1-9 – State the following: "In the example, the first CCW is stored at location X1, has m1 (IDAWs, IDAW11, IDAW12, ..., IDAW1m1), and controls the transfer of data into locations L11 to U11, L12 to U12, ... , L1m1 to U1m1. It is extremely difficult for disk adapters to handle data chained Reads with IDAWs in real time, without prefetching the entire data chain. With prefetching, the need to fetch the next CCW, and its IDAWs, in real time, are eliminated, but Read CCWs may be self-modifying. Thus, the first Read CCW which controls the reading of some number of bytes may actually modify one of the other n-1 CCWs (or their IDAWs) in the data chain. Similarly, the second Read CCW may actually modify one of the remaining n-2 CCWs (or their IDAWs), and so on")*

Neither IBM nor Jung-bae Lee teach the following limitation of Claim 16:

- waiting a period of time appropriate to prevent conflicts between transfers of bytes for the first and second read operations and to minimize the amount of time between the end of the burst transfer of data for the first read operation to the beginning of the burst transfer of data for the second read operation;

However, stating that there is a sequence in which things must occur does not change the purpose or functionality of the claimed invention.

Therefore, it would have been obvious to one of ordinary skill in the art to combine the "Integrated Circuit Devices" of Jung-bae Lee and IBM's "Bit Vector Algorithm", so that the entire system would function efficiently and accurately.

For further information, reference Ex parte Rubin , 128 USPQ 440 (Bd. App. 1959) (Prior art reference disclosing a process of making a laminated sheet wherein a base sheet is first coated with a metallic film and thereafter impregnated with a thermosetting material was held to render prima facie obvious claims directed to a process of making a laminated sheet by reversing the order of the prior art process steps.). See also In re Burhans, 154 F.2d 690, 69 USPQ 330 (CCPA 1946) (selection of any order of performing process steps is prima facie obvious in the absence of new or unexpected results); In re Gibson, 39 F.2d 975, 5 USPQ 230 (CCPA 1930) (Selection of any order of mixing ingredients is prima facie obvious.).

10. Claims 17 is rejected under 35 U.S.C.103(a) as being unpatentable over Jung-bae Lee and IBM as applied to claim 16 above, further in view of Carnevale et al. (US Patent 5,721,874).

Jung-bae Lee and IBM teach the limitations of claim 16 for the reasons above.

Jung-bae Lee's and IBM's inventions differ from the claimed invention in that there is no specific reference to checking stored information for byte sizes of cache lines.

Jung-bae Lee and IBM fail to teach claim 17, which states the following: "The method of claim 16, further comprising checking stored information concerning the size of a cache line of a cache utilized by a processor to temporarily store a copy of a subset of data stored in the memory IC in determining the quantity of bytes to which each transfer of data will be limited for both the first and second read operations." However, Carnevale states the following: "FIG. 8 is a block diagram representation illustrating a page table arrangement for storing cache characteristic information for controlling cache access to the configurable caches 12 and 22. A page table 50 stores address information. Each page table entry 52 within the page table 50 includes other page table information 54 and a cache line characteristic data 56. The cache line characteristic

data 56 includes the number of address bits to be matched in the cache directory 32 and a cache line size" (Column 4, line 50-59). Carnevale further states: "Cache characteristic information including the number of cache lines and line size to be used can be provided in a page table entry for addressing the caches 12, 22-1, 22-2, 22-3 and 22-4. Also a one-level indirection can be used from the page table to a set of cache characteristics, reducing the amount of storage needed for the characteristics. For example, four types of caching can be specified on an I/O bridge chip, and then 2 bits in the page table entry can be used to determine the cache characteristics of the cache lines corresponding to memory in that page" (Column 3, lines 52-61). Therefore, it would have been obvious to one of ordinary skill in the art to combine the "Integrated Circuit Devices" of Jung-bae Lee, the "Bit Vector Algorithm" of IBM, and Carnevale's "Configurable Cache", so that byte sizes of cache lines could be checked to improve system efficiency.

11. Claims 18 and 19 are rejected under 35 U.S.C.103(a) as being unpatentable over Jung-bae Lee and IBM as applied to claim 16 above, further in view of Kopet et al. (US Patent 5,448,310).

Jung-bae Lee and IBM teach the limitations of claim 16 for the reasons above.

Jung-bae Lee's and IBM's inventions differ from the claimed invention in that there is no specific reference to early termination.

Jung-bae Lee and IBM fail to teach claims 18 and 19, which respectively state the following: "The method of claim 16, further comprising signaling the memory IC that both the first and second read operations are to be terminated early through indications of early termination embedded in the commands transmitted to the memory IC for both the first and second read operations" and "The method of claim 16, further comprising signaling the memory

IC that both the first and second read operations are to be terminated early through transmitting first and second burst termination commands to the memory device, timed to indicate when to cease transferring further bytes of data for each of the first and second read operations." However, Kopet states the following: "The differences between Mode 1 and the Mode 0 burst read cycle shown in FIG. 31, are that for the Mode 1 cycle, HMODE is initially set high (instead of low) and there is only a single clock cycle (instead of two clocks) separating one burst access from the next. Just as for a Mode 0 burst read, however, HBRST 800 is asserted during the burst for every additional word to be accessed after the first word, and MEC 20 asserts HRDY- for every word it asserts on the data bus. However, unlike a Mode 0 burst read, Mode 1 burst reads do not require HBRST 800 to be deasserted during the last access. Also, if HBRST 800 is deasserted during a Mode 1 burst read cycle prior to reading all (BLENGTH+2) words, the burst cycle terminates on the rising edge of the next clock to follow the deassertion. Due to internal pipelining, MEC 20 reads one additional word beyond the point of termination, even though this word is never asserted onto the data bus. An example of such an "early termination," (as opposed to the "normal termination") is depicted in FIG. 33. In FIG. 33, HBRST 800 is deasserted during the HRDY- cycle for "Data 0", causing the burst to be terminated at that point. However, internally MEC 20 still reads "Data 1"" (Column 12, lines 10-34). Therefore, it would have been obvious to one of ordinary skill in the art to combine the "Integrated Circuit Devices" of Jung-bae Lee, the "Bit Vector Algorithm" of IBM, and Kopet's "Motion Estimation Coprocessor", so that early termination could occur when necessary to make the system more universally user-friendly and efficient.

12. Claim 20 is rejected under 35 U.S.C.103(a) as being unpatentable over Kopet et al., further in view of Ho Cheol Lee, Keskar et al, Carnevale et al., and the non-patent literature "Bit Vector Algorithm for Detecting Self-Data Chains" (hereafter referred to as "IBM").

Kopet teaches the following limitations of Claim 20:

> A machine-accessible medium comprising code that when executed by a processor within an electronic system, causes the electronic system to: *(Column 5, lines 40-47 – State the following: "The system of FIG. 1 operates under the control of a host processor 38, which couples to the remaining system components via bus 30. In a preferred embodiment, host processor 38 comprises a RISC processor, such as for example, an Intel i960 family processor manufactured by Intel of Santa Clara, Calif. Also coupled to bus 30 are a ROM 39 for storing host processor 38 program code and a DRAM 40")*

Ho Cheol Lee teaches the following limitations of Claim 20:

- interrogate a memory device to determine whether or not the memory device possesses banks of memory cells organized into a plurality of groups that permit independent memory operations; *(Column 13, lines 45-49 "The row control circuit is means for generating signals or clocks for selecting word lines during the time period of t.sub.RCD, developing to bit lines information data from memory cells in a read operation and precharging during the time period of t.sub.RP. In other words, the row control circuit decides whether or not the rows are open")*

Keskar teaches the following limitations of Claim 20:

- configure a memory controller to make use of a memory device that possesses such independently operable groups of banks of memory cells; *(Column 22, lines 1-8 – State that "wherein the memory controller is configured to pipeline consecutive accesses between the memory controller and a synchronous dynamic random access memory (SDRAM) to efficiently use a data bus of the SDRAM by overlapping consecutive accesses, the accesses including read and write accesses, the read and write accesses each having an activate phase followed by a command phase)*

Carnevale teaches the following limitations of Claim 20:

- check the size of a cache line of a cache utilized by a processor to temporarily store a copy of a subset of data stored in a memory device that possesses such independently operable groups of banks of memory cells; *(Column 4, line 50-59 – State the following: "FIG. 8 is a block diagram representation illustrating a page table arrangement for storing cache characteristic information for controlling cache access to the configurable caches 12 and 22. A page table 50 stores address information. Each page table entry 52 within the page table 50 includes other page table information 54 and a cache line characteristic data 56. The cache line characteristic data 56 includes the number of address bits to be matched in the cache directory 32 and a cache line size". Column 3, lines 52-61 further state: "Cache characteristic information including the number of cache lines and line size to be used can be provided in a page table entry for addressing the caches 12, 22-1, 22-2, 22-3 and 22-4. Also a one-level indirection can be used from the page table to a set of cache characteristics, reducing the amount of storage needed for the characteristics. For example, four types of caching can be specified on an I/O bridge chip, and then 2 bits in the page table entry can be used to determine the cache characteristics of the cache lines corresponding to memory in that page")*

IBM teaches the following limitation of claim 16:

- and determine a quantity of bytes to which to limit the burst transfer of bytes of data in a read transaction from a memory device that possesses such independently operable groups of banks of memory cells. *(Page 3, lines 33-45 and Page 4, lines 1-9 – State the following: "In the example, the first CCW is stored at location X1, has m1 (IDAWs, IDAW11, IDAW12, ..., IDAW1m1), and controls the transfer of data into locations L11 to U11, L12 to U12, ... , L1m1 to U1m1. It is extremely difficult for disk adapters to handle data chained Reads with IDAWs in real time, without prefetching the entire data chain. With prefetching, the need to fetch the next CCW, and its IDAWs, in real time, are eliminated, but Read CCWs may be self-modifying. Thus, the first Read CCW which controls the reading of some number of bytes may actually modify one of the other n-1 CCWs (or their IDAWs) in the data chain. Similarly, the second Read CCW may actually modify one of the remaining n-2 CCWs (or their IDAWs), and so on")*

Therefore, it would have been obvious to one of ordinary skill in the art to combine the "Motion Estimation Coprocessor" of Kopet, the "Synchronous Dynamic Random Access

Memory Devices" of Ho-Cheol Lee, the "Programmable Memory Controller" of Keskar, the "Configurable Cache" of Carnevale, and IBM's "Bit Vector Algorithm", so that the entire system would function efficiently and accurately.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lev I. Iwashko whose telephone number is (571)272-1658. The examiner can normally be reached on M-F (alternating Fridays), from 8-4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Lev Iwashko

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